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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,598	11/01/2001	Toshiya Yokogawa	5077-000073	5848

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EXAMINER	
CAO, PHAT X	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applic(s)
09/980,598	Yokogawa et al.
Examiner	**Art Unit**
Phat X. Cao	2814

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-12 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 4
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 4-12 are objected to under 37 CFR 1.75© as being in improper form because a multiple dependent claim 3. See MPEP § 608.01(n). Accordingly, the claims 4-12 have not been further treated on the merits.

Claim Rejections - 35 USC § 112

3. Claims 4-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4-12 are unclear because of their improper dependency.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4-5, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiroyuki et al (JP. 06-349860).

With respect to claims 1-2 and 4-5, Hiroyuki (Fig. 1 and abstract) discloses a semiconductor device made by providing on a substrate an active region that functions as a portion of an active element, wherein the active region is configured by layering: at least one first semiconductor layer 4 of undoped GaAs which is provided on the substrate, and at least one second semiconductor layer 5 of doped GaAs which includes a higher concentration of impurities for carriers than the first semiconductor layer 4, which has a thinner firm thickness than the first semiconductor layer 4.

Hiroyuki does not specifically disclose that the second semiconductor layer carriers can migrate to the first semiconductor layer due to quantum effects. However, because a different impurity density is set between the high doped second semiconductor layer 5 and the non-doped first semiconductor layer 4 in the channel region, the second semiconductor layer carriers would inherently migrate to the first semiconductor layer due to quantum effects.

With respect to claims 11-12, Hiroyuki's Fig. 1 further discloses: a Schottky gate electrode 8, which is in Schottky contact with a portion of the upper surface of the first semiconductor layer 4 at the uppermost portion of the active region; third semiconductor layers 7, which are provided on the active region and sandwich the Schottky gate electrode, and which

include a high concentration of impurities; and source and drain electrodes 9 being in ohmic contact with the third semiconductor layers.

6. Claims 1-2, 4-5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (JP. 5-13446).

With respect to claims 1-2 and 4-5, Suzuki (Fig. 1 and abstract) discloses a semiconductor device made by providing on a substrate 11 an active region that function as a portion of an active element, wherein the active element is configured by layering: at least one first semiconductor layer 141 of undoped GaAs which is provided on the substrate, and at least one second semiconductor layer 151 of doped GaAs which includes a higher concentration of impurities for carriers than the first semiconductor layer, which has a thickness film thickness than the first semiconductor layer.

Suzuki does not disclose that the second conductor layer carriers can migrate to the first semiconductor device due to quantum effects. However, because a different impurity density is set between the high doped second semiconductor layer and the non-doped first semiconductor layer in the active region, the second semiconductor layer carriers would inherently migrate to the first semiconductor layer due to quantum effects.

With respect to claim 12, Suzuki's Fig. 1 further disclose third semiconductor layers 221 and 222, which are provided on the active region and sandwich the Schottky gate electrode 21, and which include a high concentration of impurities, and wherein the source and drain electrodes 23 and 24 are in ohmic contact with the third semiconductor layers.

7. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Semichon et al (US. 3,739,243).

Semichon (Figs. 3 and 4) discloses a semiconductor device made by providing on a substrate 4 an active region that functions as a portion of an active element, wherein the active region is configured by layering: at least one first semiconductor layer 3 of N- GaAs (column 2, lines 40-41) which is provided on the substrate 4, and which functions as a carrier transit region; and at least one second semiconductor layer 2 of N+ GaAs (column 2, lines 40-41) which includes a higher concentration of impurities for carriers than the first semiconductor layer 3, which has a thinner film thickness than the first semiconductor layer 3, and from which carriers can migrate to the first semiconductor layer 3 due to quantum effects (see Fig. 4 and column 4, lines 4-7); wherein the concentration of impurities for carriers in the first semiconductor layer 3 is 5x10^14 atoms/cc, and the concentration of impurities for carriers in the second semiconductor layer 2 is 10^18 atoms/cc. (column 3, lines 54-60).

8. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Sumino et al (JP. 54-132173).

Sumino (Fig. 2) discloses a semiconductor device by providing on a substrate 21 an active region that functions as a portion of an active element, wherein the active region is configured by layering: at least one first semiconductor layer 22 of n type which is provided on the substrate 21, and at least one second semiconductor layer 23 of n+ type which includes a higher concentration of impurities for carriers than the first semiconductor layer 22.

Sumino does not specifically disclose that the second semiconductor layer carriers can migrate to the first semiconductor layer due to quantum effects. However, because a different impurity density is set between the high doped second semiconductor layer 23 and the low doped first semiconductor layer 22 in the active region, the second semiconductor layer carriers would inherently migrate to the first semiconductor layer due to quantum effects in forward bias condition.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumino et al in view of Odekirk (US. 6,388,272).

With respect to claims 4 and 6, Odekirk (Fig. 2) teaches the obviousness of using SiC as the material for the first and second semiconductor layers of the diode, wherein the second semiconductor layer 28 of n+ has a thickness of below 20 nm (column 9, lines 38-40). According to Odekirk, SiC would possess tremendous advantages for high temperature and high power solid state electronics (column 1, lines 24-27).

With respect to claim 7, the above combination does not disclose the thickness of the first semiconductor layer in a range as claimed. However, it would have been obvious to provide the first semiconductor layer with a thickness in the claimed range since it has been held that where the general conditions of a claim are disclosed in the prior at, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

With respect to claim 8, Sumino (Fig. 2) further discloses that the substrate 21 is a semiconductor layer that includes a high concentration of impurities, wherein the uppermost portion of the active region is made of the first semiconductor layer 24, and wherein the semiconductor device further comprises a Schottky electrode 25 providing a Schottky contact with a portion of the upper surface of the first semiconductor layer 24 at the uppermost portion of the active region.

Sumino does not disclose an electrode providing an contact with a portion of the high doped substrate 21. However, Odekirk teaches the obviousness of forming an electrode 16 in contact with the high doped semiconductor layer 28 (see Fig. 2) in order to provide an ohmic contact.

With respect to claim 3, Odekirk further teaches the obviousness of forming the concentration of impurities for carriers in the n+ second semiconductor layer 28 being 1E18/cc (column 9, lines 38-44), and the concentration of impurities for carriers in the n- first semiconductor layer 12 being less than the concentration of impurities in the n+ second semiconductor layer 28 (i.e., less than 1E18/cc).

11. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Semichon et al in view of Odekirk (US. 6,388,272).

With respect to claim 6, Odekirk (Fig. 2) teaches the obviousness of using SiC as the material for the first and second semiconductor layers of the diode, wherein the second semiconductor layer 28 of n+ has a thickness of below 20 nm (column 9, lines 38-40). According to Odekirk, SiC would possess tremendous advantages for high temperature and high power solid state electronics (column 1, lines 24-27).

With respect to claim 7, the above combination does not disclose the thickness of the first semiconductor layer in a range as claimed. However, it would have been obvious to provide the first semiconductor layer with a thickness in the claimed range since it has been held that where the general conditions of a claim are disclosed in the prior at, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PHAT X. CAO
PRIMARY EXAMINER

PC
June 30, 2002